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10CS74

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. Define computer architecture. Illustrate the seven dimensions of an ISA. **(10 Marks)**

b. Find the number of dies per 200cm wafer of circular shape that is used to cut die that is 1.5cm side and compare the number of dies produced on the same wafer if die is 1.25cm. **(06 Marks)**

c. What is dependability? Explain the two measures of dependability. **(04 Marks)**

2 a. What are the major hurdles of pipelining? Illustrate the branch hazard in detail. **(10 Marks)**

b. List and explain five ways of classifying exception in a computer system. **(05 Marks)**

c. Consider a unpipelined processor and assume that it has a 1ns clock cycle and that it uses 4 cycles for ALU operations and branches and 5 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose that due to clock skew and setup, pipelining the processor adds 0.2ns of overhead to the clock. Ignoring any latency impact, how much speedup in the instruction execution rate will be gained from a pipeline. **(05 Marks)**

3 a. List different types of data dependencies. Explain name dependences with example. **(05 Marks)**

b. Mention the drawback of 1–bit branch predictor scheme and explain the states in 2-bit predictor scheme used for dynamic branch prediction. **(05 Marks)**

c. With a neat diagram give the basic structure of Tomasulo based MIPS FP unit and explain the various field of reservation stations. **(10 Marks)**

4 a. Explain the basic VLIW approach for exploiting ILP, using multiple issues. **(10 Marks)**

b. What is branch target buffer? With the neat diagram, explain the steps when using branch target buffer for a simple five stage pipeline. **(10 Marks)**

PART – B

5 a. Explain the different taxonomy of parallel architecture. **(04 Marks)**

b. With neat diagrams, explain the basic structure of centralized shared memory and distributed shared memory multiprocessor. **(06 Marks)**

c. Explain the directory based cache coherence for a distributed memory multiprocessor system along with the state transition diagram. **(10 Marks)**

6 a. Explain the organization of the data cache in the AMD opteron microprocessor. **(05 Marks)**

b. Explain the techniques for fast address translation. **(05 Marks)**

c. List and explain six basic cache optimization techniques. **(10 Marks)**

7 a. List eleven advanced optimizations of cache performance and explain any five in detail. **(12 Marks)**

b. Explain memory technology and optimizations. **(08 Marks)**

8 a. Explain detecting and enhancing loop level parallelism for VLIW. **(10 Marks)**

b. Explain Intel IA – 64 architecture in detail. **(10 Marks)**

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